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NOISE-REDUCING TRANSISTOR ARRANGEMENT

Cross-Reference To Related Application

This application is a nation stage of International Patent Application Serial No. PCT/DE2004/002657, filed December 3, 2004, which published in German on June 30, 2005 as WO/2005/060099, and is incorporated herein by reference in its entirety.

Field of the Invention

The invention relates to a noise-reducing transistor arrangement, an integrated circuit, and a method for reducing the noise of field effect transistors.

Background of the Invention

The noise of a field effect transistor (in particular MOSFET, "metal oxide semiconductor field effect transistor") limits the accuracy of an electrical circuit. This is problematic particularly when a signal having a small amplitude occurs in such a circuit. Therefore, the performance of an analog circuit, in particular, is limited by the phenomenon of noise.

The low-frequency noise of a MOS transistor is caused by statistical loading or unloading of defect states in particular at the interface between the channel region and the gate insulating region of the field effect transistor. At low frequencies, this mechanism supplies the dominant contribution to the noise. On account of their localization the defects are also often referred to as interface states. Predominantly those defects whose energy level lies close to the (quasi) Fermi level of the charge carriers contributing to the current flow contribute to the low-frequency noise. Other interface states whose energy level is significantly higher or lower are either completely occupied or completely unoccupied and thus do not contribute to the noise, cf. S. Christensson, I. Lundström, and C. Svensson, "Low frequency noise in MOS transistors – I theory," Solid-St. El. 11, pp. 791-812, 1968.